The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DONG YEUNG KWAK

Appeal No. 2003-2178
Application No. 09/660,186

ON BRIEF

Before GARRIS, WALTZ, and DELMENDO, Administrative Patent Judges.

DELMENDO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal under 35 U.S.C. § 134 (2003) from the examiner's final rejection of claims 2 through 7 and 9 through 20 (final Office action mailed Aug. 9, 2002, paper 8), which are all of the claims pending in the above-identified application.

The subject matter on appeal relates to a thin film transistor liquid crystal display (TFT LCD). Further details of

this appealed subject matter are recited in representative claims 2, 9, and 15 reproduced below:

2. A TFT LCD (thin film transistor liquid crystal display) comprising:
a first substrate and a second substrate;
a scanning line on the first substrate;
a signal line formed to cross the scanning line, wherein the signal line does not include an extension pattern;
a channel layer formed along the signal line and extended to a portion of the scanning line;
source and drain electrodes formed separated on the channel layer over the scanning line;
a pixel electrode connected to the drain electrode; and
a liquid crystal layer formed between the first substrate and the second substrate;
wherein the drain electrode is parallel to the signal line.

9. A TFT LCD comprising:
a first substrate and a second substrate;
a plurality of scanning lines on the first substrate;
a gate insulating layer on an entire surface inclusive of the scanning lines;
a channel layer on the gate insulating layer to cross the scanning lines having a portion extended to a top of at least one of the plurality of scanning lines;
source and drain electrodes formed separated on the channel layer over the scanning lines;
a signal line formed as a unit with the source electrode along the channel layer which is formed to cross the scanning lines, wherein the signal line does not include an extension pattern;
a protection film formed on an entire surface inclusive of the signal line;
a pixel electrode connected to the drain electrode on the protection film; and,

a liquid crystal layer formed between the first substrate and the second substrate;

wherein the drain electrode is parallel to the signal line.

15. A TFT LCD having a first substrate, a second substrate, and liquid crystal sealed between the first and second substrates, comprising:

a scanning line on the first substrate;

a gate insulating layer on the scanning line;

a channel layer on the gate insulating layer;

a signal line formed to cross the scanning line to cover a portion of the channel layer, wherein the signal line does not include an extension pattern;

a drain electrode formed on the channel layer spaced a distance away from the signal line in parallel to the signal line;

a protection film formed on an entire surface of the first substrate inclusive of the drain electrode; and

a pixel electrode formed on the protection film connected to the drain electrode;

wherein the drain electrode is parallel to the signal line.

The examiner relies on the following prior art reference as evidence of unpatentability:

Ono et al. (Ono)	6,377,323 B1 (effective filing date Jul. 19, 1996)	Apr. 23, 2002

Claims 2 and 4 through 7 on appeal stand rejected under 35 U.S.C. § 102(e) as anticipated by Ono. (Examiner's answer mailed Apr. 29, 2003, paper 15, pages 3-5.) Also, claims 3 and 9 through 20 on appeal stand rejected under 35 U.S.C. § 103(a) as unpatentable over Ono. (Id. at 5-8.)

We affirm both rejections. Because we are in substantial agreement with the examiner's factual findings and legal conclusions as set forth in the answer, we adopt them as our own and add the following comments for emphasis.[1]

As pointed out by the examiner (answer at 3-4), Ono describes a TFT LCD comprising: a first substrate SUB1; a second substrate SUB2; a gate line GL (i.e., a scanning signal line) disposed on the first substrate SUB1; parallel data lines (i.e., video signal lines) DL; an i-type semiconductor layer (i.e., a channel layer); source and drain electrodes SD1 and DL, respectively, separated on the semiconductor layer over the gate line GL; a pixel electrode ITO1; and a liquid crystal layer LC between the first and second substrates SUB1 and SUB2. (Figures 2 and 3; column 1, line 64 to column 2, line 57; column 3, line 38 to column 4, line 64.)

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[1] The appellant's statement regarding the grouping of claims lacks clarity. (Appeal brief filed Feb. 24, 2003, paper 14, p. 4.) We also emphasize that "[m]erely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable." See 37 CFR § 1.192(c)(7)(2003)(effective Dec. 1, 1997). Nevertheless, in our discussion of each of the two grounds of rejection, we will consider the claims separately to the extent that they have been separately argued within the meaning of the regulation.

The appellant does not specifically dispute the examiner's factual findings that Ono's video signal line DL is formed to cross the scanning line GL and that the signal line DL does not include an extension pattern. Nor does the appellant specifically contest the examiner's findings that the channel layer AS is formed along the signal line DL and extended to a portion of the scanning line GL. Rather, the appellant's main argument is "that the drain electrode in the cited reference is not over the scanning line, parallel to the signal line, and connected to the pixel electrode." (Appeal brief at 5.)

The appellant's argument lacks discernible merit. Ono teaches that a portion of the data line constitutes the drain electrode. (Column 4, lines 43-46.) In Figure 3, Ono's source and drain electrodes SD1 and DL are shown as being separated on the channel layer (i.e., the semiconductor layer AS) and disposed over the gate line GL (i.e., the scanning signal line). Relying on Ono's disclosure at column 4, lines 56-64, the examiner reasons that Ono's drain electrode would inherently or necessarily be connected to the pixel electrode when the polarities are reversed during operation. (Answer at 4.) The appellant does not refute this reasoning. With respect to the drain electrode being parallel to the signal line, nothing

substantiates the appellant's allegation that Ono's source/drain electrode would not be parallel to the signal line. Accordingly, the examiner correctly held that, prima facie, Ono describes each and every limitation recited in appealed claim 2.[2] In re Schreiber, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997).

While the appellant alleges that the claimed invention provides certain "advantages" (appeal brief at 6), there is not a shred of evidence to support such an allegation. Moreover, the "advantages," even if established, cannot constitute a factual basis to overcome a rejection under 35 U.S.C. § 102. In re Malagari, 499 F.2d 1297, 1302, 182 USPQ 549, 553 (CCPA 1974).

For these reasons, we uphold the examiner's 35 U.S.C. § 102(e) rejection of appealed claims 2 and 4 through 7 as anticipated by Ono.

As to the examiner's 35 U.S.C. § 103(a) rejection, the appellant argues that Ono "does not teach a channel layer on the gate insulating layer to cross the scanning lines having a portion extended to a top of at least one of the plurality of scanning lines as recited by claim 9." (Appeal brief at 8.)

[2] We limit our discussion to appealed claim 2 because the appellant does not argue the claims separately with respect to

Further, the appellant urges that the reference "does not teach a drain electrode formed on the channel layer spaced a distance away from the signal line in parallel to the signal line as recited by claim 15." (Id.) These arguments are also unpersuasive because the appellant offers no explanation as to why the examiner's findings to the contrary are in error.

Lastly, the appellant alleges that the claimed invention solves a newly discovered problem. (Appeal brief at 9.) Again, however, there is no objective evidence (e.g., experimental evidence) to substantiate the allegation that the claimed invention solves any problem whereas Ono's TFT LCD does not.

For these reasons, we also uphold the examiner's 35 U.S.C. § 103(a) rejection of appealed claims 3 and 9 through 20 as unpatentable over Ono.

In summary, we affirm the examiner's rejections under: (i) 35 U.S.C. § 102(e) of appealed claims 2 and 4 through 7 as anticipated by Ono; and (ii) 35 U.S.C. § 103(a) of appealed claims 3 and 9 through 20 as unpatentable over Ono.

The decision of the examiner is affirmed.

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the examiner's 35 U.S.C. § 102(e) rejection.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

Bradley R. Garris)
Administrative Patent Judge)
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Thomas A. Waltz)
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) APPEALS AND
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